What is claimed is:

1. A compander comprising
an input signal,
gain calculate logic responsive to the input signal for calculating a gain calculate signal,
synchronizer logic responsive to the input signal and the gain calculate signal for synchronizing the input signal and the gain calculate signal to provide an output signal.

2. The compander of claim 1 wherein the synchronizer logic includes a gain cell.

3. The compander of claim 2 wherein the synchronizer logic further includes a synchronizer block.

4. The compander of claim 3 wherein the synchronizer block provides a gain signal and a delayed signal to the gain cell, and the gain cell output is the output signal.

5. The compander of claim 1 wherein the gain calculate logic includes detection logic for detecting a predetermined condition of the input signal, and wherein the gain calculate signal is generated only after the predetermined condition of the input signal occurs.

6. The compander of claim 5 wherein the predetermined condition of the input signal includes a zero crossing.

7. The compander of claim 6 wherein the predetermined condition of the input signal further includes a failure to have a zero crossing within a predetermined period.

8. The compander of claim 5 further including
monitor logic for monitoring the input signal,
power estimator logic responsive to the monitor logic for providing the gain calculate signal.

9. The compander of claim 8 wherein the monitor logic initiates monitoring on the occurrence of the predetermined condition.

10. The compander of claim 8 wherein the monitor logic terminates monitoring on the occurrence of the predetermined condition.

11. The compander of claim 9 wherein the monitor logic generates a signal value and periodically passes the stored signal value to the power estimator logic.

12. The compander of claim 10 wherein the monitor logic generates a signal value and passes the generated signal value to the power estimator logic upon occurrence of the predetermined condition.

13. The compander of claim 11 wherein the generated signal value is the peak signal.

14. The compander of claim 11 wherein the generated signal is the average signal.

15. The compander of claim 11 wherein the generated signal is the RMS signal.

16. The compander of claim 12 wherein the generated signal is the peak signal.

17. The compander of claim 12 wherein the generated signal is the average signal.

18. The compander of claim 12 wherein the generated signal is the RMS signal.

19. The compander of claim 12 wherein the monitor logic resets upon occurrence of the predetermined condition.

20. The compander of claim 8 wherein the power estimator logic includes initial power estimator logic for determining an intial power estimate, and

variable attack and release logic responsive to the initial power estimate for determining a rate of change for the gain calculate signal.

21. The compander of claim 20 wherein the initial power estimate includes a plurality of initial power estimates.

22. The compander of claim 21 wherein the variable attack and release logic comprises a plurality of variable attack and release modules.

23. The compander of claim 20 wherein the initial power estimator logic provides at least first and second power estimator signals, and wherein the variable attack and release logic compares the first power estimator signal with the second power estimator signal.

24. The compander of claim 20 wherein the initial power estimator logic provides at least one power estimator signal to the variable attack and release logic, and the output of the variable attack and release logic is fed back to provide a second input to the variable attack and release logic.

25. The compander of claim 23 wherein the second power estimator signal is provided by preliminary power estimator logic which receives as an input the output of the variable attack and release logic.

26. The compander of claim 25 wherein the preliminary power estimator logic receives as an additional input the input signal.

27. An equalizer comprising

a first input representative of a time betweeen events,

a computation engine responsive to the input and capable of supplying an equalization value in accordance with the first input,

a second input representative of a signal characteristic associated with the time between events, and

combiner logic for combining the equalization value with the second input.

28. The equalizer of claim 27 wherein the computation engine is a lookup table.

29. The equalizer of claim 27 wherein the computation engine is a processor .

30. The equalizer of claim 29 wherein the processor includes an algorithm to perform an appropriate computation for the computation engine.

31. The equalizer of claim 29 wherein the processor includes digital logic.

32. The equalizer of claim 30 wherein the algorithm includes a plurality of computer program steps.

33. The equalizer of claim 27 wherein a plurality of the second inputs is received during the time between events.

34. A signal processor comprising
a first input representative of a time betweeen events,
a computation engine responsive to the input and capable of supplying filter parameters in accordance with the first input,
a second input representative of a signal characteristic associated with the time between events, and
a filter responsive to the filter parameters for processing the second input.

35. The signal processor of claim 34 wherein the filter includes a plurality of filters.

36. The signal processor of claim 35 wherein the second input includes a plurality of inputs and each of the plurality of filters responds to an associated one of the plurality of inputs.

37. The signal processor of claim 34 wherein the second input is equalized.

38. The signal processor of claim 34 wherein the computation engine is a lookup table.

39. The signal processor of claim 34 wherein the computation engine is a processor.

40. The signal processor of claim 34 wherein the processor includes an

algorithm to perform an appropriate computation for the computation engine.

41. The signal processor of claim 39 wherein the processor includes digital logic.

42. The signal processor of claim 40 wherein the algorithm includes a plurality of computer program steps.

43. The signal processor of claim 34 wherein a plurality of the second inputs is received during the time between events.

44. A compander having
an input comprising at least one power estimator signal,
first signal processing stage for processing the at least one power estimator signal.

45. The compander of claim 44 wherein the processing is demodulating.

46. The compander of claim 44 wherein the processing is filtering.

47. The compander of claim 44 wherein the at least one power estimator signal is a plurality of power estimator signals.

48. The compander of claim 47 wherein the processing is combining of at least some of the plurality of power estimator signals.

49. The compander of claim 47 wherein the processing is selecting a preferred one of the plurality of power estimator signals.

50. A compander having
a first input comprising at least one local power estimator signal,
a second input comprising at least one external power estimator signal,
a first signal processor for processing the first input and the second input to produce a first output.

51. The compander of claim 50 wherein the processing includes combining the

first and second inputs.

52. The compander of claim 50 wherein the processing includes selecting one of the first and second inputs.

53. The compander of claim 50 wherein the processing includes scaling at least one of the first and second inputs.

54. The compander of claim 50 wherein the second input comprises a plurality of external power estimator signals, and further including a second signal processor for processing the plurality of external power estimator signals to produce a single output signal to the first signal processor.

55. The compander of claim 54 wherein the processing performed by the second signal processor includes combining at least some of the plurality of external power estimator signals.

56. The compander of claim 54 wherein the processing performed by the second signal processor includes selecting among at least some of the plurality of external power estimator signals.

57. The compander of claim 54 wherein the processing performed by the second signal processor includes scaling at least one of the plurality of external power estimator signals.

58. The compander of claim 54 wherein the processing performed by the second signal processor includes demodulating at least one of the plurality of external power estimator signals.

59. The compander of claim 54 wherein the processing performed by the second signal processor includes filtering at least one of the plurality of external power estimator signals.

60. The compander of claim 50 wherein the first input comprises a plurality of local power estimator signals, and further including a third signal processor for processing the plurality of local power estimator signals to produce an exported power estimator signal.

61. The compander of claim 60 wherein the third signal processor comprises a plurality of signal processors, each of which produces an exported power estimator signal.

62. The compander of claim 60 wherein the processing performed by the third signal processor includes combining at least some of the plurality of local power estimator signals.

63. The compander of claim 60 wherein the processing performed by the third signal processor includes selecting among at least some of the plurality of local power estimator signals.

64. The compander of claim 60 wherein the processing performed by the third signal processor includes scaling at least one of the plurality of local power estimator signals.

65. The compander of claim 60 wherein the processing performed by the third signal processor includes modulating at least one of the plurality of local power estimator signals.

66. The compander of claim 60 wherein the processing performed by the third signal processor includes filtering at least one of the plurality of local power estimator signals.

67. The compander of claim 50 further including a second signal processor for processing the second input signal and a third signal processor for processing the first input signal to produce an exported power estimator signal.

68. 25. The compander of claim 67 wherein the second input comprises a plurality of local power estimator signals and the second signal processor processes at least one of the local power estimator signals to produce a single output signal to the first signal processor.

69. The compander of claim 68 wherein the first input comprises a plurality of local power estimator signal , and the third signal processor processes the plurality of local power estimator signals to produce an exported power estimator signal.

70. The compander of 67 wherein the processing performed by the second signal processor includes demodulating the second input signal, and the processing performed by the third signal processor including modulating the first input signal.

71. The compander of claim 68 wherein the processing performed by the second and third signal processors is selected from a group including modulating, demodulating, scaling, selecting, combining and filtering.

72. A signal processing method for use with companders comprising the steps of
providing at least one local power estimator signal,
providing at least one external power estimator signal,
signal processing the local power estimator signal and the external power estimator signal to produce a first output.

73. The signal processing method of claim 72 wherein the external power estimator signal comprises a plurality of secondary external power estimator signals, and further including the step of signal processing the plurality of secondary external power estimator signals to produce the external power estimator signal.

74. A compander having
a first plurality of power estimator signals,
first signal processing stage for combining at least some of the first plurality of power estimator signals and for generating at least one output signal.

75. A compander having
a first external power estimator signal,
a second external power estimator signal,
a first signal processor for processing the first and second power estimator signals to produce a first output wherein processing includes at least one of a group comprising scaling, combining and selecting the first and second power estimator signals.

76. The compander of claim 75 wherein the processing includes demodulating at least one of the external power estimator signals.

77. The compander of claim 75 wherein the processing includes scaling at least one of the external power estimator signals.

78. The compander of claim 75 wherein the processing includes filtering at least one of the external power estimator signals.

79. The compander of claim 75 further including a second signal processor for processing the first output.

80. The compander of claim 79 wherein the second signal processor modulates the first output.

81. The compander of claim 79 wherein the second signal processor scales the first output.

82. The compander of claim 79 wherein the second signal processor filters the first output.